# STRUCTURE OF TFT PLANAR DISPLAY PANEL

## FIELD OF THE INVENTION

The present invention relates to a structure of a planar display panel, and more particularly to a structure of a thin film transistor (TFT) planar display panel. The present invention also relates to a process for manufacturing a structure of a thin film transistor (TFT) planar display panel.

## BACKGROUND OF THE INVENTION

Due to the progress in manufacturing technology, liquid crystal displays (LCDs) are expected to take the place of conventional cathode-ray-tube (CRT) displays to become a leader in the display field in the near future. A thin film transistor (TFT) LCD is particularly popular among them. Please refer to FIG. **1** which is a schematic circuit diagram showing a pixel unit of a conventional TFT-LCD. The pixel unit includes a TFT switching unit **11**, a liquid crystal displaying unit **12** and a storage capacitor **13**. The storage capacitor **13** is connected to the liquid crystal displaying unit **12**, which also functions as a capacitor, in parallel as a backup of the liquid crystal displaying unit **12** to store charges. Thus, the rapid voltage drop rate of the liquid crystal displaying unit **12** occurring when the TFT **11** turns off can be avoided.

FIGS. **2**A–**2**C are schematic cross-sectional diagrams illustrating the steps of a conventional process for producing a low temperature poly silicon thin film transistor (LTPS-TFT) of a TFT-LCD. Please refer to FIG. **2**A. A buffer layer **21**, for example made of silicon dioxide, is formed on a glass substrate **20**. An intrinsic amorphous silicon (i-a-Si) layer is formed on the buffer layer **21**, and then converted into an intrinsic polycrystalline silicon (i-poly-Si) layer **22** by a laser crystallization. A photoresist mask structure **23** is formed on the top of the i-poly-Si layer **22** by a masking and micro-photolithographic procedure. Subsequently, the portion of the i-poly-Si layer **22** exposed from the photoresist mask structure **23** is processed by an N-type implantation procedure with for example arsenic (As) or phosphorous (P) dopants to form source/drain regions **221** of an N-channel TFT.

Please refer to FIG. **2**B. After the photo-mask **23** is removed, an insulating layer, for example made of silicon dioxide, is provided on the resulting substrate to form a gate insulator **24**. Subsequently, a gate conductive layer is applied on the gate insulator **24** by sputtering, and a gate conductive structure **25** is formed by another masking and micro-photolithographic procedure. The gate conductive structure **25** is used as a mask in the following implantation procedure to provide trace N-type dopants in the i-poly-Si layer **22**. Thus, lightly doped drain (LDD) regions **222** are formed with an N-channel **28** therebetween.

Afterwards, an interlayer dielectric **26** is applied onto the top of the resulting substrate, and contact holes **261** are defined at the proper positions. Then, a metal conductive layer is formed by sputtering, and fills the contact holes **261** to define a source/drain connecting line structure **27**.

Since the LTPS-TFT has a modified TFT structure, that is, it is changed from a bottom gate structure to a top gate structure, the LTPS-TFT has better device properties. Unfortunately, such a top-gate LTPS-TFT structure has a disadvantage resulting from the exposed channel **28** under the back light. When the LTPS-TFT is in an OFF condition, significant photoelectric current will be generated in the channel area **28** due to the illumination of the back light source. In this situation, the current leakage of the device increases, and errors are likely to occur to adversely affect the gray-scale change of the liquid crystal and deteriorate the quality of the display.



Therefore, the purpose of the present invention is to develop a structure of a thin film transistor (TFT) planar display panel and a process for manufacturing the TFT planar display panel to deal with the above situations encountered in the prior art.

## SUMMARY OF THE INVENTION

An object of the present invention is to provide a TFT-LCD panel structure and a process for producing the TFT-LCD panel structure for efficiently reducing the generation of the photoelectric current in the channel region of the top-gate TFT structure and avoiding the current leakage of the devices.

According to an aspect of the present invention, there is provided a structure of a thin film transistor (TFT) planar display panel. The structure includes a light-transmissible substrate, a buffer layer formed on the light-transmissible substrate, a top-gate TFT structure formed on the buffer layer and including a channel region, and a light-shielding structure formed between a back light source and the top-gate TFT structure, and substantially aligned with the channel region for protecting the channel region from illumination of the back light source.

For example, the light-transmissible substrate can be a glass substrate.

For example, the buffer layer can be formed of silicon nitride, silicon oxide, or a combination thereof.

In an embodiment, the light-shielding structure is formed between the back light source and the buffer layer.

In an alternative embodiment, the light-shielding structure is formed in the buffer layer.

Preferably, the light-shielding structure is formed of an opaque material having a relatively high melting point. For example, the light-shielding structure is formed of chromium (Cr), molybdenum (Mo), tungsten (W) or organic material.

Preferably, the top-gate TFT structure includes a semiconductor layer formed on the buffer layer and formed therein the channel region and source/drain regions, a gate insulating structure formed on the semiconductor layer, a gate conductive structure formed on the gate insulating structure above the channel region, a dielectric layer formed on the gate conductive structure and the gate insulating structure, and a conductive line structure formed on the dielectric layer and penetrating through the gate insulating structure and the dielectric layer to contact with the source/drain regions in the semiconductor layer.

Preferably, the structure further includes lightly doped drain regions disposed next to the source/drain regions and sandwiching therebetween the channel region.

For example, the semiconductor layer can be a polycrystalline silicon layer.

Preferably, the gate conductive structure is formed of chromium (Cr), tungsten molybdenum (WMo), tantalum (Ta), aluminum (Al) or copper (Cu).

For example, the gate insulating structure can be formed of silicon oxide.

Preferably, the structure further includes a black matrix which is implemented by the light-shielding structure.